REMARKS

Claims 1-7 were pending in the application at the time of this office action. Claims 1-7 have been amended. Claim 8 has been added. Thus, claims 1-8 are present for examination. Reexamination and reconsideration of the application in view of the following remarks are requested.

The examiner requested that applicant make certain corrections to the specification. Applicant has made the requested corrections.

The examiner objected to claim 4 and requested that applicant make certain corrections to claim 4. Applicant has made appropriate corrections to claim 4.

Claims 1-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over applicant's admitted prior art in view of Watt, U.S. Patent No. 5701024. The examiner correctly notes that applicant's admitted prior art does not teach a first conductive type well under the first diffusion layer, having a lower dopant concentration than the first diffusion layer. The examiner states, however, that Watt teaches in Figure 5 a first conductive type well 54 under a first diffusion layer 44, having a lower dopant concentration than the first diffusion layer. The examiner also states that it would have been obvious to a person of ordinary skill in the art to combine the references, applicant's admitted prior art and Watt, "in order to reduce contact spiking during ESD event." Office Action, page 4.

The examiner's rejection of claims 1-7 is respectfully traversed because the prior art of record does not teach all of the claim limitations. For example, Watt teaches a first conductive type well (N-well) 54 under a first diffusion layer (n+ drain region) 44, in which the first diffusion layer 44 is connected to an input terminal V_{PAD} via contact 68. Applicant discloses, on the other hand, that the first diffusion layer (n+ source region) 3c, under which the first conductive type well (N-well) 1a is formed, should never be connected to an input terminal 7. Fig. 2 shows that the second diffusion layer is connected to the input terminal 7. Indeed, claim 1 recites that the first diffusion layer 3c is connected to a reference potential 9 rather than to the input terminal 7. Claim 1 further recites that the second diffusion region is connected to the input terminal 7.

Thus, since the prior art of record does not teach each of the claim limitations, the PTO has not established a *prima facie* case of obviousness under 35 U.S.C. § 103.

Moreover, applicant believes that it would not have been obvious to combine the references because Watt uses the first conductive type well in a different manner than Applicant. First, Watt suggests that the first conductive type well (N-well) should be formed under an n+ drain region, which in Watt, is connected to the input terminal. As discussed above, Applicant's claim 1 recites the first diffusion region being connected to ground rather than to an input terminal. Neither applicant's admitted prior art, nor Watt, provide a motivation or suggestion for combining the references.

In addition, as illustrated in applicant's Figure 5, and as described in the specification at pages 21 and 22, applicant's inclusion of the well 1a of second conductive type improves the performance of the semiconductor device when a positively polarized surge is confronted. Applicant's employment of the well 1a accomplishes this by raising the electric potential of an adjacent base region (2 in Fig. 5) following a breakdown in the drain region (3b in Fig. 5) above the adjacent base region. Specifically, referring to Fig. 5, when the voltage exceeds a certain value, breakdown takes place in the vicinity of the drain region 3b. After the breakdown, a current flows from the drain region 3b to the well 2 which results in turning on an NPN parasitic bipolar transistor. Because the current generated due to the breakdown starts flowing along the current path illustrated in Fig. 5, the potential of the base region 2 of the parasitic bipolar transistor readily increases. The advantages of applicant's configuration are further discussed in the specification and are illustrated in applicant's Fig. 4.

Watt, on the other hand, describes that its well 54 of a second conductive type is disposed to "wholly underlie" drain region 44 under contact 68. Watt, col. 8, lns. 9-16. Watt states that the well 54 of a second conductive type helps to prevent contact spiking during the ESD event by increasing the depth of the junction under the contact 68. Watt describes that the well 54 of the second conductive type "accomplishes this object by increasing the depth of the junction under the contacts thereby increasing the distance that a spike would have to propagate in order to short out the junction itself." Watt, col. 5, lns. 35-41. Accordingly, Watt's explanation for inclusion of the well 54 is

to prevent a spike from damaging the contact above the well. Watt does not contemplate, nor does Watt teach, utilizing the well to facilitate raising the electric potential of an adjacent base region following a breakdown in a drain region above the base region. Conversely, applicant is not concerned with protecting a contact above the well from a spike.

To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to those skilled in the art, to modify the reference or to combine reference teachings. In re Vaeck, 947 F.2d 488, 20 USPQ 2d 1438 (Fed. Cir. 1991). There is no motivation or suggestion in applicant's admitted prior art or in Watt to combine the references. As such, the PTO has not established a *prima facie* case of obviousness under 35 U.S.C. § 103. The examiner's rejection of claim 1 is respectfully traversed. Since Claims 2 and 3 are dependent on claim 1, the examiner's rejection of those claims is likewise traversed.

Claim 8 has been added. Claim 8 adds the feature that the first conductive type well partially underlies an element isolation film. Applicant believes that claim 8 is further distinguished from the prior art of record.

Independent claim 4 recites the same feature discussed above with respect to claim 1. Accordingly, the examiner's rejection of claim 4 is respectfully traversed. Since claims 5-7 are dependent on claim 4, the examiner's rejection of those claims is likewise traversed.

Claim 6 recites a dopant high-concentration region that is beneath the second conductive type well wherein the bottom of the region extends no lower than the bottom of the well of the first conductive type. The examiner states that applicant's admitted prior art teaches a dopant high concentration region 20 (the semiconductor substrate) that is beneath the second conductive type well. Applicant's admitted prior art does not disclose, however, a first conductive type well, nor does it disclose a first conductive type well being formed at the same depth as the bottom of the region 20, the semiconductor substrate. Accordingly, Claim 6 recites features that are neither

disclosed nor suggested in the prior art of record. The examiner's rejection of Claim 6 is respectfully traversed.

With respect to claims 5 and 6, the Examiner stated that Morihisa, J.P. 10-173070, teaches in Fig. 2 a first conductive type well 5' under the first diffusion layer 16, wherein the bottom of the first conductive type well 5' is at the same depth as the bottom of the second conductive type well 5 or at a level deeper than the bottom of the second conductive type well. However, Morihisa teaches in Fig. 2a output 143 being connected to drain 116 of NMOS 152 having a first conductive type well (N-well) 105', while V_{in} is connected to an impurity region 117 of protective resistance element 153. Thus, Morihisa's configuration is distinct from Applicant's. Moreover, there is no motivation or suggestion to combine the features of Applicant's admitted prior art, Watt, and Morihisa. Accordingly, the Examiner's rejections based on Morihisa are respectfully traversed.

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance. Re-examination and reconsideration of the application, as amended, an allowance of the claims at an early date is respectfully requested.

Respectfully submitted,

Date: December 18, 2001

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yasuyuki MORISHITA

Title: SEMICONDUCTOR DEVICE

Appl. No.: 09/621,614

Filing Date: 07/21/00

Examiner: Nadav, Ori

Art Unit: 2811

MARKED-UP COPY OF AMENDMENT AND REQUEST FOR RECONSIDERATION UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Box Non-Fee Amendment
Washington, D.C. 20231

Sir:

In reply to the Office Action dated September 26, 2001, please amend the above-identified application as follows:

In the Specification:

On page 1, paragraph beginning at line 11, delete and insert the following:

In a semiconductor integrated circuit device, an input protection circuit section or an output protection circuit section (referred to as an input/output protection circuit section, hereinafter) is set between an input terminal or an output terminal ~~or an output terminal~~(referred to as an input/output terminal, hereinafter) and an internal circuit in order to protect circuit elements inside from failure which may be brought about by an ESD or the like applied to the input/output terminal.

On page 17, paragraph beginning at line 21, delete and insert the following:

Fig. 8 is a schematic cross-sectional view showing a protection circuit section of ~~an~~ a Comparative Example.

In the Claims:

1. (Amended) A semiconductor device having an input/output protection circuit section on a semiconductor substrate~~:~~, wherein:

said input/output protection circuit section comprises a plurality of field effect transistors connected in parallel, each of which has a first ~~and second~~ diffusion ~~layers~~ layer of a first conductive type and a second diffusion layer of the first conductive type and a gate electrode that is ~~set in the region sandwiched~~ disposed between ~~these~~ said first and second diffusion layers; ~~and~~

a dopant diffusion region of a second conductive type that is set at a distance from ~~the region where~~ said plurality of field effect transistors ~~are formed; and~~;

~~while~~ wherein said dopant diffusion region is connected ~~with~~ to a reference potential, and wherein the second diffusion layer is connected ~~with~~ to an input/output terminal section; and

wherein under the first diffusion layer, there is formed a first conductive type well with a lower dopant concentration than the first diffusion layer.

2. (Amended) The semiconductor device according to Claim 1, wherein said gate electrode and said dopant diffusion region of second conductive type are ~~placed~~ disposed over ~~the~~ a second conductive type well that is formed on the surface of the semiconductor substrate; and wherein the bottom of said first conductive type well is formed at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well.

3. (Amended) The semiconductor device according to Claim 1, wherein said plurality of field effect transistors are N-channel type field effect transistors.

4. (Amended) A semiconductor device having, on a semiconductor substrate, an input/output protection circuit section that contains a complementary field effect transistor~~:~~, wherein:

said complementary field effect transistor ~~is composed of~~ comprises a first field effect transistor having a first ~~and second~~ diffusion ~~layers~~ layer of first conductive type, a second diffusion layer of first conductive type, and a gate electrode that is ~~set in the region sandwiched~~ disposed between these layers and a second field

effect transistor having a third ~~and fourth~~ diffusion ~~layers~~ layer of second conductive type, a fourth diffusion layer of second conductive type, and a gate electrode that is ~~set in the region sandwiched~~ disposed between these layers;

~~and~~ wherein a first dopant diffusion region of second conductive type is set at a distance from ~~the region where~~ said first field effect transistor ~~is formed~~, and a second dopant diffusion region of first conductive type is set at a distance from ~~the region where~~ said second field effect transistor ~~is formed; and~~;

wherein the first dopant diffusion region is connected ~~with~~ to a first reference potential~~;~~, the second dopant diffusion region~~, with~~ is connected to a second reference potential~~;~~, and the second diffusion layer and the fourth diffusion layer are each connected ~~with~~ to an input/output terminal section; and

wherein under the first diffusion layer, there is formed a first conductive type well with a lower dopant concentration than the first diffusion layer.

5. (Amended) The semiconductor device according to Claim 4, wherein the gate electrode of the first field effect transistor and the first dopant diffusion region are ~~placed~~ disposed over ~~the~~ a second conductive type well that is formed on the surface of the semiconductor substrate; and

wherein the bottom of said first conductive type well is formed at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well.

6. (Amended) The semiconductor device according to Claim 5, wherein, beneath the second conductive type well, there is set a dopant high-concentration region containing second conductive type dopants with a higher dopant concentration than the second conductive type well; and

wherein the bottom of said first conductive type well is formed at the same depth as the bottom of said dopant high-concentration region or at a level deeper than the bottom of said dopant high-concentration region.

7. (Amended) The semiconductor device according to Claim 4, wherein the first field effect transistor is an N-channel type field effect transistor.